IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent Application of)
)

OGASAWARA et al.)   **Art Unit 2655**
)

Application Number: 10/806,128)
)

Filed: March 23, 2004)
)

For: DISK ARRAY SYSTEM)
)

Attorney Docket No. ASAM.0116)

Honorable Assistant Commissioner
  for Patents
Washington, D.C. 20231

PETITION TO MAKE SPECIAL UNDER 37 C.F.R. § 1.102(d)

FOR ACCELERATED EXAMINATION

Sir:

Pursuant to 37 C.F.R. § 1.102(d), Applicant respectively requests the application to be examined on the merits in conjunction with the pre-examination search results, the detailed discussion of the relevance of the results and amendments as filed concurrently.

Substantive consideration of the claims is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicant's undersigned representative at the address and telephone number indicated below.

Respectfully submitted,

02/03/2005 AWONDAF1 00000149 10806128
01 FC:1464   130.00 OP

Stanley P. Fisher
Registration Number 24,344

Juan Carlos A. Marquez
Registration Number 34,072

REED SMITH LLP
3110 Fairview Park Drive, Suite 1400
Falls Church, Virginia 22042
(703) 641-4200
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SPF/JCM/JT

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STATEMENTS & PRE-EXAMINATION SEARCH REPORT
SUPPLEMENTAL TO
THE PETITION TO MAKE SPECIAL

Sir:

   Pursuant to 37 C.F.R. §§ 1.102 and MPEP 708.02 VIII, Applicant hereby submits that (1) all claims of record are directed to a single invention, or if the Office determines that all the claims presented are not obviously directed to a single invention, will make an election without traverse as a prerequisite to the grant of special status; (2) a pre-examination search has been conducted according to the following field of search; (3) copies of each reference deemed most closely related to the subject matter encompassed by the claims are enclosed; and (4) a detailed discussion of the references pointing out how the claimed subject matter is patentable over the references is also enclosed herewith.

FIELD OF THE SEARCH

   A search was conducted with the US Patent Office's full-text of US patent databases in the following *US Manual of Classification* subclasses:

Class	Subclasses	Description
709		**ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MULTICOMPUTER DATA TRANSFERRING OR PLURAL PROCESSOR SYNCHRONIZATION**
	214	.. Plural shared memories
	220	. Network computer configuring
	223	. Computer network managing
	245	. Computer-to-computer data addressing
711/		**ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY**
	111	.. Accessing dynamic storage device
	112	...Direct access storage device (DASD)
	147	. Shared memory area
	162	...Backup

The search was directed to an array system comprising: a plurality of storage devices for storing data; a storage device control unit for controlling storage of data in the plurality of storage devices; a connection unit being connected with the storage devices; a plurality of first channel control units each having a first processor of converting file data, received through an local area network outside the disk array system itself, into block data and requiring storage of the data in the plurality of storage devices and a second processor of transferring the block data to the plurality of storage devices through the connection unit and the storage device control unit in response to the request sent from the first processor, and the plurality of first channel control units being connected with the connection unit and the local area network; a shared memory for storing control information to be transferred between the plurality of first channel control units and the storage device control unit; and a cache memory for temporarily saving data to be transferred between the plurality of first channel control units and the storage device control unit. The second processor located in each the plurality of first channel control units divides a plurality of storage areas in the plurality of storage devices for storing the block data and a processor information storage area for storing

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processor information regarding a processing state of each of the first processors to be transferred among the plurality of the first processors through the use of the plurality of storage areas of the storage devices. The storage device control unit copies the processor information stored in the processor information storage area into a backing up storage area.

LIST OF RELEVANT REFERENCES

The search revealed the following U.S. patents, which are listed for convenience:

U.S. Patent No.	Inventor
6,081,883	Popelka et al.

U.S. Pat. App. Pub. No.	Inventor	US filing date	Pub. Date
2003/0191904 A1	Iwami et al.		
2003/0204580 A1	Baldwin et al.		
2004/0128456 A1	Kobayashi et al.	April 29, 2003	July 1, 2004
2004/0148329 A1	Ogasawara et al.	Sep. 30, 2003	July 29, 2004

Discussion of References:

US Pat. No. 6,081,883 to **Popelka** is assigned to Auspex Systems and entitled "Processing System with Dynamically Allocatable Buffer Memory." **Popelka** describes a scalable file server that has a host processor, one or more function specific processors, including network processors and file storage processors. Network processors may monitor the status of the host processor 105. Each of the file processors 130 is connected in turn to a storage processor 140 to form a file processor 150 (col. 6, lines 9-11). Each of the storage processors is connected to disks. Each of the storage processors further has a write cache 141 which buffers write requests to respective disk drives (col. 2, lines 36-38; col. 5, lines 19-21 and 45-55). However, **Popelka**'s system structure shown in Fig. 1 is essentially different form Fig. 1 of the invention as now recited in claim 1. In addition, **Popelka** only backs-up files (col. 3, line 53), rather than any "processor information regarding a processing state of each of said first processors 112 to be transferred among said plurality of said first processors 112." As such, **Popelka** does not provide "a second processor located in each said plurality of first channel control units divides a plurality of storage areas in said plurality of storage devices for storing said block data and a processor information storage area for storing

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processor information regarding a processing state of each of said first processors to be transferred among said plurality of said first processors through the use of said plurality of storage areas of said storage devices" and "a storage device control unit copies said processor information stored in said processor information storage area into a backing up storage area" as now recited in claim 1 of the present invention.

US Pat. App. Pub. No. 2004/0128456 of **Kobayashi** et al. is assigned to Hitachi, Ltd. and entitled "Storage System of and Data Backup Method for the Same." **Kobayashi** (Fig. 1) has a first/share memory 147, a second/cache memory 148, ONE disk adapter 130, a connection mechanism, and a disk array 122. The network adapter 130 includes a first port 131, and a first/NAS processor 132 and a second/ I/O processor 133. The first processor 132 receives a file access request and gives instructions to access the data stored in the disks 123. The second processor 133 transfers access to the data stored in the storage disks 123 to the second/cache memory (paragraphs 8 and 34). However, **Kobayashi** has ONE disk adapter 130, rather than "a plurality of first channel control units each having a first processor of converting file data, received through an local area network outside said disk array system itself, into block data and requiring storage of said data in said plurality of storage devices and a second processor of transferring said block data to said plurality of storage devices through said connection unit and said storage device control unit in response to said request sent from said first processor, and said plurality of first channel control units being connected with said connection unit and said local area network" as now recited in claim 1 of the present invention. In addition. the I/O processor 133 transfers backup instructions for the data stored in the storage device to the shared memory 147, and sends out data stored in the storage device to the device storing backup data (Abstract). **Kobayashi** only stores backed-up data of data stored in the storage devices 300, rather than any "processor information regarding a processing state of each of said first processors 112 to be transferred among said plurality of said first processors 112." As such, **Kobayashi** does not provide "a second processor located in each said plurality of first channel control units divides a plurality of storage areas in said plurality of storage devices for storing said block data and a processor information storage area for storing processor information regarding a processing state of each of said first processors to be transferred among said plurality of said first processors through the use of said plurality of storage areas of said storage devices" and "a storage device control unit copies said processor information stored in said processor information

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storage area into a backing up storage area" as now recited in claim 1 of the present invention.

US Pat. App. Pub. No. 2004/0148329 of **Ogasawara** et al. is assigned to Hitachi, Ltd. entitled "Storage Device System and Storage Device System Activating Method." **Ogasawara** describes a storage device capable of being connected to a plurality of networks, and its storage device system may be comprised of a communication control section including, a first processor that converts information of a first form into information of a second form and a second processor that accesses plurality of storage devices via the connection unit (paragraphs 9 and 10). Although **Ogasawara** contains similar figures and two common inventors, **Ogasawara's** backup devices 900, 910 stores backed-up data of data stored in the storage devices 300, when the information processing system communicates with the storage device control system 100 over the SAN 500 or the LAN 400 (paragraphs 36 & 45), rather than any "processor information regarding a processing state of each of said first processors 112 to be transferred among said plurality of said first processors 112." As such, **Ogasawara** does not provide "a second processor located in each said plurality of first channel control units divides a plurality of storage areas in said plurality of storage devices for storing said block data and a processor information storage area for storing processor information regarding a processing state of each of said first processors to be transferred among said plurality of said first processors through the use of said plurality of storage areas of said storage devices" and "a storage device control unit copies said processor information stored in said processor information storage area into a backing up storage area" as now recited in claim 1 of the present invention.

US Pat. App. Pub. No. 2003/0191904 of **Iwami** is entitled "Computer System having Plural of Storage Systems." **Iwami** provides the background of networks 110 that may be of the same type for each server connected thereto or may be of mutually different types for the respective servers (paragraph 36). **Iwami**'s system structure shown in Fig. 1 is different form Fig. 1 of the invention as now recited in claim 1. In addition, **Iwami** does not backs-up anything. As such, **Iwami** does not provide "a second processor located in each said plurality of first channel control units divides a plurality of storage areas in said plurality of storage devices for storing said block data and a processor information storage area for storing processor information regarding a processing state of each of said first processors to be transferred among said plurality of said first processors through the use of said plurality of

storage areas of said storage devices" and "a storage device control unit copies said processor information stored in said processor information storage area into a backing up storage area" as now recited in claim 1 of the present invention.

US Pat. App. Pub. No. 2003/0204580 of **Baldwin** et al. is entitled "Methods and Apparatus for Management of Mixed Protocol Storage Area Networks." Discussed is a first set of hosts connected to a first network manager and a second set of components that is likewise coupled to a second network manager. The second network manager may transmit to the first network manager information regarding at least one component in the second set and providing with that information an identifier of the type used by the first network manager in referring to components of the first set (paragraph 8). **Baldwin**'s system structure shown in Fig. 1 is different form Fig. 1 of the invention as now recited in claim 1. In addition, **Baldwin** does not backs-up anything. As such, **Baldwin** does not provide "a second processor located in each said plurality of first channel control units divides a plurality of storage areas in said plurality of storage devices for storing said block data and a processor information storage area for storing processor information regarding a processing state of each of said first processors to be transferred among said plurality of said first processors through the use of said plurality of storage areas of said storage devices" and "a storage device control unit copies said processor information stored in said processor information storage area into a backing up storage area" as now recited in claim 1 of the present invention.

CONCLUSION

Based on the results of the comprehensive prior art search as discussed above, Applicants contend that the position calculation method as now recited in independent claim 1, especially the features of "a second processor 119 located in each said plurality of first channel control units divides a plurality of storage areas in said plurality of storage devices 300 for storing said block data and a processor information storage area for storing processor information regarding a processing state of each of said first processors 112 to be transferred among said plurality of said first processors 112 through the use of said plurality of storage areas of said storage devices 300" and "a storage device control unit 100 copies said processor information stored in said processor information storage area into a backing up storage area" are patentably distinct from the cited prior art references.

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In particular, the disk array system 600, as recited now in claim 1 (e.g., Fig. 1), comprising: a plurality of storage devices 300 for storing data; a storage device control unit 100 for controlling storage of data in said plurality of storage devices 300; a connection unit 150 being connected with said storage devices 300; a plurality of first channel control units CHAs 110 (e.g., Fig. 7) each having a first processor 112 of converting file data, received through an local area network 400 outside said disk array system 600 itself, into block data and requiring storage of said data in said plurality of storage devices 300 and a second processor 119 of transferring said block data to said plurality of storage devices 300 through said connection unit 150 and said storage device control unit 100 in response to said request sent from said first processor 112, and said plurality of first channel control units 110 being connected with said connection unit 150 and said local area network 400; a shared memory 120 for storing control information to be transferred between said plurality of first channel control units 110 and said storage device control unit 100; and a cache memory 130 for temporarily saving data to be transferred between said plurality of first channel control units 110 and said storage device control unit 100. The second processor 119 located in each said plurality of first channel control units divides a plurality of storage areas in said plurality of storage devices 300 for storing said block data and a processor information storage area for storing processor information regarding a processing state of each of said first processors 112 to be transferred among said plurality of said first processors 112 through the use of said plurality of storage areas of said storage devices 300. The storage device control unit 100 copies said processor information stored in said processor information storage area into a backing up storage area (p. 5, last three lines).

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art references, Applicant respectfully contends that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable consideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance

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of the above-captioned application, the Examiner is invited to contact the Applicant's undersigned representative at the address and phone number indicated below.

Respectfully submitted,

_____
Stanley P. Fisher
Registration Number 24,344

_____
Juan Carlos A. Marquez
Registration Number 34,072

REED SMITH LLP
3110 Fairview Park Drive
Suite 1400
Falls Church, Virginia 22042
(703) 641-4200

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SPF/JCM/JT